What is claim d is:

Fig. 1 1. A modulator comprising:

a PLL circuit (110) which detects a phase difference between an input signal and a reference signal,

an AGC circuit (140) which controls a gain of a modulating signal (130) and outputs a control signal (output of 140), and

a voltage controlled oscillation circuit (120) which controls an oscillation frequency of a signal outputted from said PLL circuit based on said control signal,

wherein said voltage controlled oscillation circuit (120) includes:

a first voltage controlled reactance unit (121) which inputs said signal outputted from said PLL circuit (110),

a second voltage controlled reactance unit (122) which inputs said control signal, and

a high-frequency oscillation circuit (124) connected in parallel with said first and second voltage controlled reactance units, which outputs said input signal.

2. The modulator as claimed in Claim 1, wherein the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, wherein the cathodes of the first varactor diode and second varactor diode are connected each other, and the signal outputted from the PLL circuit is inputted

where the cathodes are connected each other.

3. The modulator as claimed in Claim 2, wherein the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, wherein the cathodes of the third varactor diode and fourth varactor diode are connected each other, and the control signal is inputted where the cathodes are connected each other.

4. The modulator as claimed in Claim 2 or Claim 3, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

5. The modulator as claimed in Claim 4, wherein the AGC circuit outputs the control signal on the basis of the frequency divided signal.

6. The modulator as claimed in Claim 2 or Claim 3, wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.

7. The modulator as claimed in Claim 1, wherein the first voltage controlled reactance unit includes a first varactor diode and a first capacitor, wherein the cathode of the first varactor diode is connected to one end of the first capacitor, and the signal outputted from the PLL circuit is inputted where the cathode and the one end are connected each other.

8. The modulator as claimed in Claim 2, wherein the second voltage controlled reactance unit includes a second varactor diode and a second capacitor, wherein the cathode of the second varactor diode is connected to one end of the second capacitor, and the control signal is inputted where the cathode and the one end are connected each other.

9. The modulator as claimed in Claim 7 or Claim 8, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

10. The modulator as claimed in Claim 9, wherein the AGC circuit outputs the control signal on the basis of the frequency divided signal.

11. The modulator as claimed in Claim 7 or Claim 8, wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.

12. A modulator comprising:

a PLL circuit that detects a phase difference between an input signal and a reference signal,

a selection circuit that outputs control signals on the basis of a signal outputted from the PLL circuit, and

a voltage controlled oscillation circuit that controls an oscillation frequency of the signal outputted from the PLL circuit on the basis of the control signal,

wherein the voltage controlled oscillation circuit includes:

a first voltage controlled reactance unit that inputs the signal outputted from the PLL circuit,

second and third voltage controlled reactance units that input the control signals, and

a high-frequency oscillation circuit connected in parallel with the first, second, and third voltage controlled reactance units, which outputs the input signal.

13. The modulator as claimed in Claim 12, wherein:

the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, in which the cathodes of the first varactor diode and second varactor diode are connected each other, and the signal outputted from the PLL circuit is inputted where the cathodes are connected each other;

the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, in which the cathodes of the third varactor diode and fourth varactor diode are connected each other, and the control signal is inputted where the cathodes are connected each other; and

the third voltage controlled reactance unit includes a fifth varactor diode and a sixth varactor diode, in which the cathodes of the fifth varactor diode and sixth varactor diode are connected each other, and the control signal is inputted where the cathodes are connected each other.

14.The modulator as claimed in Claim 13, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

15. The modulator as claimed in Claim 13, wherein the selection circuit outputs the control signal to the second voltage controlled reactance unit, when a voltage level of the signal outputted from the PLL circuit is higher than a threshold level, and outputs the control signal to the second and third voltage controlled reactance units, when the voltage level of the signal outputted from the PLL circuit is lower than the threshold level.

Fig. 6

16. A modulator comprising:

a PLL circuit that compares phases of a reference signal and a frequency divided signal in which a frequency of an input signal is divided, and outputs a phase difference signal,

a selection circuit that outputs control signals on the basis of the frequency divided signal, and

a voltage controlled oscillation circuit that controls an oscillation frequency of the phase difference signal on the basis of the control signal,

wherein the voltage controlled oscillation circuit includes:

a first voltage controlled reactance unit that inputs the phase difference signal,

second and third voltage controlled reactance units that input the control signals, and

a high-frequency oscillation circuit connected in parallel with the first, second, and third voltage controlled reactance units, which outputs the input signal.

17. The modulator as claimed in Claim 16, wherein:

the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, in which the cathodes of the first varactor diode and second varactor diode are connected each other, and the phase difference signal is inputted where the cathodes are connected each other;

the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, in which the cathodes of the third varactor diode and fourth varactor diode are connected each other, and the control signal is inputted where the cathodes are connected each other; and

the third voltage controlled reactance unit includes a fifth varactor diode and a sixth varactor diode, in which the cathodes of the fifth varactor diode and sixth varactor diode are connected each other, and the control signal is inputted where the cathodes are connected each other.

18. The modulator as claimed in Claim 17, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides

the frequency of the input signal to output the frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

19. The modulator as claimed in Claim 17, wherein the selection circuit outputs the control signal to the second voltage controlled reactance unit, when a voltage level of the phase difference signal is higher than a threshold level, and outputs the control signal to the second and third voltage controlled reactance units, when the voltage level of the phase difference signal is lower than the threshold level.